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Temperature dependence of electrical properties in In/$Cu_2ZnSnTe_4$/Si/Ag diodes

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Abstract. $Cu_2ZnSnTe_4$ (CZTTe) thin films with In metal contact were deposited by thermal evaporation on monocrystalline n-type Si wafers with Ag ohmic contact to investigate the device characteristics of an In/CZTTe/Si/Ag diode. The variation in electrical characteristics of the diode was analysed by carrying out current–voltage (I–V) measurements in the temperature range of 220–360 K. The forward bias I–V behaviour was modelled according to the thermionic emission (TE) theory to obtain main diode parameters. In addition, the experimental data were detailed by taking into account the presence of an interfacial layer and possible dominant current transport mechanisms were studied under analysis of ideality factor, n. Strong effects of temperature were observed on zero-bias barrier height (Φ_{B0}) and n values due to barrier height inhomogeneity at the interface. The anomaly observed in the analysis of TE was modelled by Gaussian distribution (GD) of barrier heights with 0.844 eV mean barrier height and 0.132 V standard deviation. According to the Tung's theoretical approach, a linear correlation between Φ_{B0} and n cannot be satisfied, and thus the modified Richardson plot was used to determine Richardson constant (A^*). As a result, A^* was calculated approximately as 120.6 A cm^{-2} K^{-2} very close to the theoretical value for n-Si. In addition, the effects of series resistance (R_s) by estimating from Cheng's function and density of surface states (N_{ss}) by taking the bias dependence of effective barrier height, were discussed.

Keywords. Temperature dependence; I–V characteristics; barrier inhomogeneity; Gaussian distribution; series resistance.

1. Introduction

The family of I_2–II–IV–VI_4 quaternary structures composed of earth-abundant, low-cost and non-toxic elements has attracted much attention in recent years due to several optical and electrical applications [1–4]. Among these materials, Cu-based, Cu_2–II–IV–VI_4 compounds in a large family of group-II elements with Zn and Cd; and group-IV elements with Ge and Sn, have potential for electronic applications [3–7]. In the search for an environment-friendly and low-cost material, quaternary compounds have been employed to tailor their electronic characteristics for the possible diode applications [1–10]. The study of electronic transport mechanisms across heterostructures has been point of interest as a field of research and potential device applications. The current can flow in a diode with the charge transport along the junction modelled by different carrier transport mechanisms as thermionic emission (TE) over the barrier, tunnelling through the barrier and carrier generation/recombination at the junction interface. In this case, with the assumption on TE, diode parameters, such as ideality factor, barrier height, series resistance that affects mostly the performance of the device, are extracted for information on the nature of the diode. In addition to room temperature analysis, it is necessary to determine these parameters in a wide range of working temperatures to detail the nature of barrier and conduction mechanisms. Most of the experimental studies were reported on the deviation from ideal diode characteristics, and these works were focused on the anomaly in the current transport mechanism and pre-dominant mechanism on this process. In this case, the performance and reliability of these diodes were discussed with effects of oxide/dielectric interface layer or assuming the presence of an insulating layer. These interfaces are an essential part of the formation of electronic and optoelectronic devices in which the characteristics of barrier height dominate electronic transport and device operation. In the literature, thin film layers have been triggered interest on the metal–semiconductor, metal–insulator–semiconductor and metal–oxide–semiconductor applications in which the observed barrier inhomogeneities are related to non-linearity in temperature dependence of barrier height and ideality factor [3,4]. Among them, in thin film technology, Te-based

compounds in this family have been less studied than their sulphide and selenide counterparts [6–10]. Most of the works on thin films in the form of $Cu_2ZnSnTe_4$ (CZTTe) were concentrated on their thermo-electric characteristics [6–9]. Herein we studied, for the first time to our knowledge, diode characteristics in tetrahedrally coordinated quaternary CZTTe thin films deposited by DC/RF sputtering using stacked precursors on a one-sided polished n-Si wafer substrate. In fact, among the Cu_2ZnSnX_4 group of compounds, it was reported that the distribution of Cu, Zn and Sn can cause negligibly small differences in the material properties as band structures, electronic characteristics [9]. Experimentally, similar to S- and Se-based compounds, the structure of this new compound was reported with point group symmetry $I\bar{4}2m$ and the lattice parameters of 0.6088 and 1.2180 nm [1,8].

In this work, the less studied kesterite CZTTe structure has been employed to offer an extensive field for Te-based material design which is expected to be similar to compounds with S and Se, and to trigger efforts on new materials for commercially competitive kesterite photovoltaics. Therefore, I–V properties of the heterostructure were investigated to understand diode characteristics and also to extract the main diode parameters under the effect of diode temperature. As a result of observed I–V behaviour in the fabricated diode; by means of difference in carrier concentration of layers, current conduction in the diode can be modelled under the effect of inhomogeneous barrier formation.

2. Experimental

In this study, the CZTTe thin films were prepared by sequential-sputtering from elemental and compound targets of Cu, SnTe and ZnTe by using a three-magnetron DC/RF sputtering system. To obtain a stoichiometric and homogeneous film structure, the thickness of each layer of the samples was monitored and controlled *in situ* by using an Inficon XTM/2 deposition monitor. CZTTe thin films were fabricated on soda-lime glass to investigate the material properties and also on single-side polished mono-crystalline n-type Si (111) wafers having the resistivity of 5–10 (Ω cm) substrates to construct the diode structure. Before the deposition, the back surface of the Si substrate was coated with Ag and then annealed at 400°C to form an ohmic contact for electrical measurements. In the deposition process, the chamber pressure was lowered to around 10^{-7} Torr before the substrate heating process and subsequently maintained at about 6×10^{-3} Torr after introducing pure Ar gas for the generation of plasma. During the sputtering, the substrate temperature was maintained at about 200°C. The deposition procedure, the material properties and uniformity of the film layer were controlled *via* conducting several deposition trials, and the results showed that the technique has a capability of producing film samples with similar characteristics.

The thickness of the films deposited on both glass and Si substrates was measured by using a Vecoo Dektak 6 M profilometer and it was found to be around 400 nm. Crystal structure of the films was investigated by using a Rigaku Miniflex X-ray diffraction (XRD) system equipped with a CuKα radiation source having the average wavelength of 1.54 Å. Transmission and reflection measurements were carried out by using a Bentham PVE 300 system at room temperature and then, optical transition characteristics and band structures were investigated. A QUANTA 400F field emission scanning electron microscope (SEM) equipped with energy dispersive X-ray spectroscopy (EDS) facility was used for imaging film surface and analysis of the elemental concentration in the film layer. For the electrical analysis, room temperature resistivity measurements were performed *via* I–V measurements according to the four-point probe method in which current was supplied by using a Keithley 220 programmable current source, and voltage was measured by using a Keithley 619 electrometer/multimeter. The diode structure was completed by thermal evaporation of an In metal contact on the film layer deposited on the n-Si wafer and 100°C post-annealing treatment for the diode to increase the adhesion of the contact to the surface. For temperature dependent I–V measurements, the electrical connection was provided on In front and Ag back contacts, and the computer-controlled measurement setup including a Keithley 2401 sourcemeter, model 22 CTI Cryodyne closed-cycle helium refrigeration system and LakeShore DSC-91C temperature controller was used.

3. Results and discussion

From EDS measurements, the relative atomic percentage of the constituent elements CZTTe thin film layer was obtained as Cu:Zn:Sn:Te = 13:10:21:56% by considering the expected experimental errors of about 1%. In figure 1, XRD measurement of the film sample on a glass substrate showed that the as-grown film layer is in a polycrystalline structure with the main orientation along the (112) plane direction [7,8]. As given in figure 1, the XRD pattern of the deposited film is consistent with the JCPDS cards 01-081-5256 and 01-081-7520, and also with the literature works which indicate the obtained CZTTe profile possibly in the kesterite phase [6,8].

The surface morphology of the deposited CZTTe film layer was analysed by using SEM measurements (figure 2). From the SEM micrograph recorded for this layer, crack-free and uniform film deposition was obtained without any observable defects on the film surface. The optical characteristics of the CZTTe structure were analysed by using the samples deposited on the glass substrates. From the room temperature transmission measurements given in figure 3, the absorption coefficient of this structure was calculated as about 10^4 cm^{-1} in the visible region which makes the CZTTe material suitable for light absorbing application. According to the assumption on the direct band gap transition behaviour, band gap of the

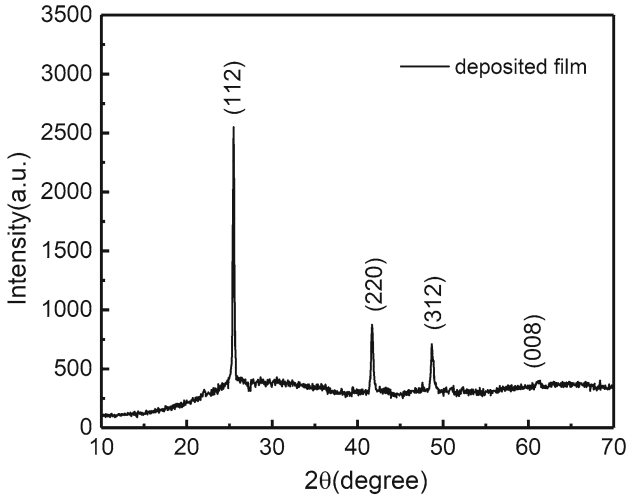

Figure 1. XRD profile of the CZTTe thin film layer.

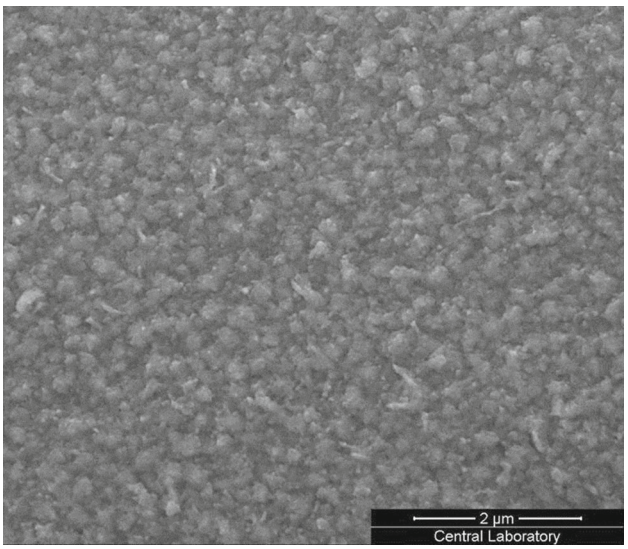

Figure 2. SEM micrograph of the CZTTe thin film layer.

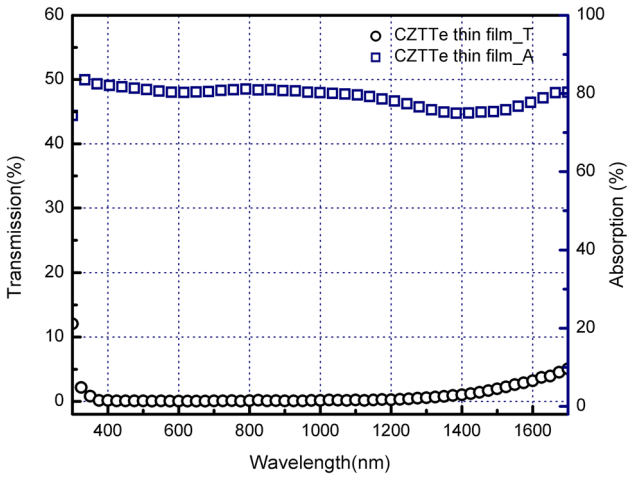

Figure 3. Spectral transmission and absorption curves of the CZTTe thin film layer.

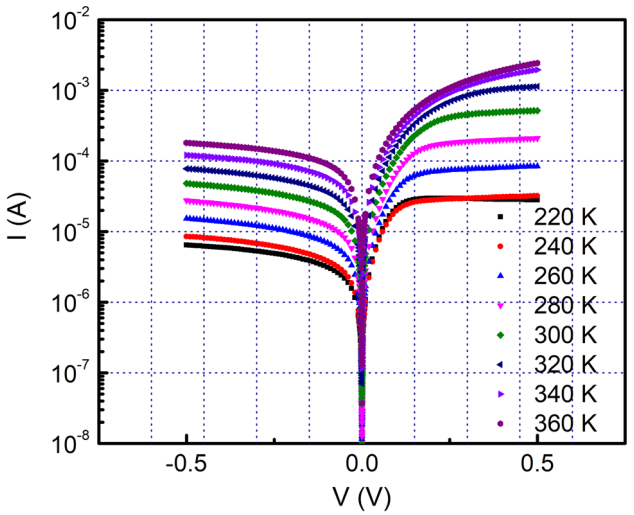

Figure 4. I–V characteristics of the In/CZTTe/Si/Ag structure at different ambient temperatures.

thin film was found as about 1.1 eV which might be originated from the fabrication methods and compositional variations in the structure with the literature. The measurement of the electrical properties by the four-point probe method at room temperature showed that it had a sheet resistance of about $10^6\ \Omega\ \mathrm{sq}^{-1}$.

The fabricated heterostructure was characterized under the results of temperature dependent I–V measurements. According to this analysis, diode parameters were calculated as a function of sample temperature and possible conduction mechanisms were analysed. The experimental semi-logarithmic forward bias I–V curve of the In/CZTTe/Si/Ag sandwich structure is given in figure 4 in the temperature range of 220–360 K. As seen from this figure, the deposited structure shows a rectifying behaviour in the studied voltage range [11,12]. The rectification factor (RF), which is the ratio of I_F/I_R, forward and reverse currents, was calculated as about 10^1 in magnitude for all studied temperatures.

In the ideal case, the current flow across the junction through the Schottky barrier can be evaluated according to the TE model. However, for the forward bias case, the experimental I–V curve should be analysed under the consideration of a deviation from linearity with the effect of series resistance R_s as in the following relation [13,14]:

$$I = I_0\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \quad (1)$$

where I_0 is the reverse saturation current, q is the electronic charge, V is the applied forward bias voltage, IR_s term is the voltage drop under the effect of R_s, n is the ideality factor of the diode, k is the Boltzmann constant and T is the absolute diode temperature. The linear region in the

Table 1. Electrical parameters of the In/CZTTe/Si/Ag diode.

T(K)	n	I_0 (A)	Φ_{B0} (eV)	N_{ss} (10^{13} eV^{-1} cm^{-2})
220	2.941	3.61×10^{-6}	0.439	2.604
240	2.702	5.30×10^{-6}	0.497	2.283
260	2.528	9.17×10^{-6}	0.515	2.049
280	2.382	1.29×10^{-5}	0.547	1.853
300	2.246	1.98×10^{-5}	0.575	1.671
320	2.175	3.09×10^{-5}	0.601	1.577
340	2.114	4.54×10^{-5}	0.639	1.494
360	2.055	6.04×10^{-5}	0.658	1.415

semi-logarithmic plot (figure 4) was chosen as a region of interest to neglect the voltage drop across R_s [12] and also the case of $V > 3kT/q$ was applied to neglect the reverse current contribution [11,15,16] in the usage of equation (1) for the analysis of the diode parameters. In equation (1) with assumption of the TE model, I_0 was parametrized with an effective diode area, A, sample temperature, T and zero-bias barrier height of the junction Φ_{B0} as:

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{B0}}{kT}\right) \tag{2}$$

where A^* is the effective Richardson constant given as, $A^* = 4\pi qm^*k^2/h^3 = 120\,(m^*/m)$ (A cm^{-2} K^{-2}) [12]. Here, m is the mass of majority carrier and m^* is its constant effective mass value; thus for n-type Si, A^* is approximated as 120 (A cm^{-2} K^{-2}) [11]. In this study, experimentally, I_0 values were obtained by the straight line of extrapolated intercept of the semi-logarithmic I–V curve at the zero bias ($V = 0$) at the current axis. Then, Φ_{B0} values were calculated using I_0 values according to equation (2) and both results as a function of the sample temperature are listed in table 1.

The deviation from the standard diode behaviour was investigated by calculating ideality factor, n, according to the following relation:

$$n(T) = \frac{q}{kT}\left(\frac{\mathrm{d}(V)}{\mathrm{dln}(I)}\right). \tag{3}$$

In figure 4, the exponential behaviour in the I–V relation may be deviated for higher forward bias voltages, and so that due to the effect of R_s, saturation behaviour is expected in the semi-logarithmic plot. The voltage drop across resistance can be related to the contact resistance between the metal and the semiconductor and resistivity nature of the semiconductor. The effects of R_s can be neglected over the voltage drop on the rectifying barrier with working in the linear forward bias region below saturation as shown in figure 4 [17]. As a result of this relation, n values were found at each studied temperature from the slope of the linear region of the I–V plot and are tabulated in table 1.

From the experimental results shown in figure 5 at various temperatures, Φ_{B0} values were found to decrease, whereas n

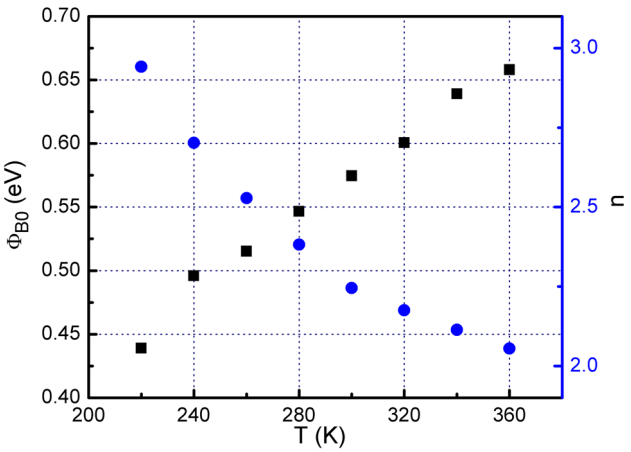

Figure 5. The variation in the Φ_{B0} and n of the In/CZTTe/Si/Ag diode with temperature.

values increase with decreasing temperature. This variation in n and Φ_{B0} depending on temperature can be evaluated as a deviation from the pure TE model. It may occur as a result of inhomogeneous barrier height formation by the presence of the interfacial layer and also non-uniformity of the interfacial charges and recombination current through the interfacial states of the junction [13,14,18]. In addition, the temperature dependence of both Φ_{B0} and n values is illustrated in figure 6. From this figure, the obtained n and Φ_{B0} values were observed in a linear correlation between each other. Based on the Tung's theoretical approach, the extrapolation of the Φ_{B0} values to $n = 1$ was found as 0.89 eV different from the band gap value of n-Si, so that this result can also be indicative for the deviation from the TE to model current transport mechanism in the diode [11,16].

Since the obtained temperature dependent n values are not close to unity, a modified TE transport model could be estimated for this diode structure [19]. Therefore, the transport model was determined as anomaly in TE with the effect of the insulator layer at the junction interface and particular distribution of interface states localized in this region [20–23]. From the evaluation of the barrier height Φ_{B0} by using equation (2), the Richardson plot of saturation current was found in a non-linear behaviour as observed from $\ln(I_0/T^2)$

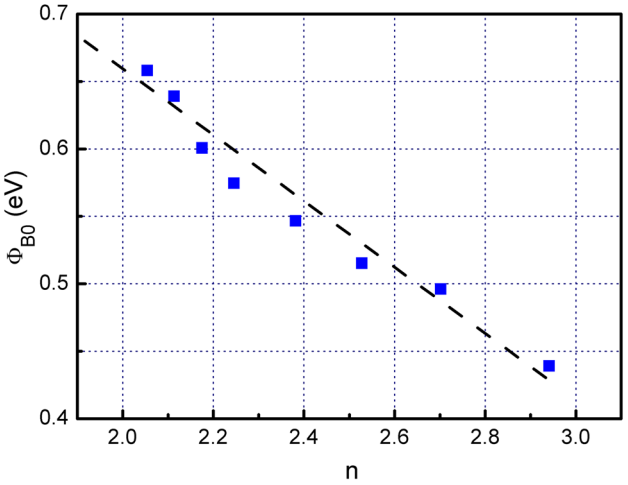

Figure 6. Φ_{B0} *vs.* n plot of the In/CZTTe/Si/Ag diode.

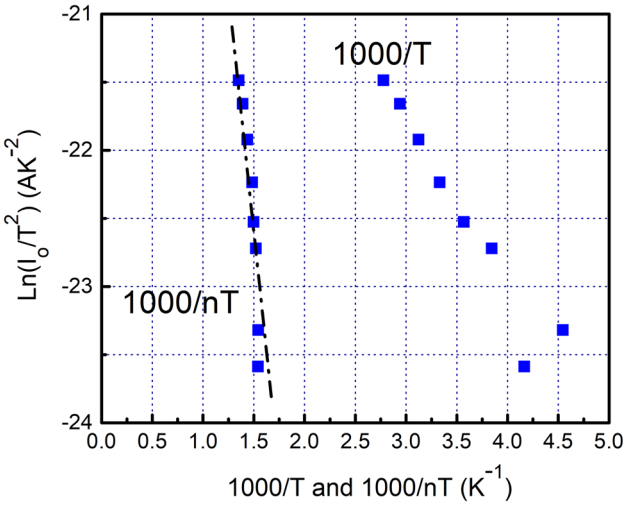

Figure 7. Richardson plot of the In/CZTTe/Si/Ag diode.

vs. $1000/T$ (figure 7). Theoretically, it is expected as in a linear relation [17], however it was found to be more linear by plotting $\ln(I_0/T^2)$ *vs.* $1000/nT$ (figure 7). Based on temperature-dependence of Φ_{B0} and n, this characteristic can be discussed as inhomogeneity in the barrier height and it might be related to the inhomogeneities in the interfacial layer composition, the interfacial charges and the interfacial layer thickness [24–26]. Thus, in order to indicate these variations in the barrier height, the I_0 expression can be re-written as [13,14,27,28]:

$$I_0 = AA^* \exp\left(-a\chi^{1/2}\delta\right) \exp\left(-\frac{q\Phi_{\text{Beff}}}{nkT}\right) \tag{4}$$

where Φ_{Beff} is the effective barrier height potential and $a\chi^{1/2}\delta$ is the hole tunnelling factor with the parameters with constant $a = (4\pi/h)(2m^*)^{1/2}$, mean tunnelling barrier presented by the interfacial insulator layer, χ and the thickness of the interfacial film through the carriers tunnel, δ.

The assumption on the modified I_0 given in equation (4) can be applicable in the bias region where the effect of the reverse current can be neglected. Therefore, for the applied forward bias values higher than $3kT/q$, the temperature dependence in n and Φ_{B0} can be evaluated by using this relation. From equation (4), modified barrier height, Φ_{Beff} was determined at the extrapolation of the straight line in the $\ln(I_0/T^2)$ *vs.* $1000/nT$ plot, and it was found as 0.522 eV. In addition, the Richardson constant was calculated as 1.722 A cm^{-2} K^{-2}, which is a highly deviated result from the expected values [11].

Generally, the initial assumptions on the deviation from the standard diode behaviour resulted in the effects of an insulating interface layer between the metal contact and semiconductor film layer, the density of the interface states (N_{ss}) and also R_s. In this case, R_s is considerably effective for the downward behaviour in the semi-logarithmic I–V curve; however the effect of N_{ss} is observable in both linear and non-linear regions of the forward bias I–V characteristics [27]. The high forward bias I–V–T dependence of the diode was observed as a deviation from the exponential behaviour under the effect of these parameters. Thus, the range of the linear region dependent on the N_{ss} and R_s can be increased by lowering both of these parameters [29]. Although barrier height and ideality factor were calculated from the low forward bias region according to the TE model, device parameters such as R_s, barrier height and ideality factor can be determined by using the procedure developed by Cheung and Cheung [30]. The obtained results in the barrier height and ideality factor may not be more accurate with increasing this linear region. However, in the high current range where the I–V characteristics are not linear, Cheung's functions described as:

$$\frac{dV}{d\ln(I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{5}$$

and

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{6}$$

can be used to investigate temperature dependent R_s values, where $H(I) = q\Phi_B + IR_s$, Φ_B is the barrier height obtained from the downward curvature of the forward I–V region. In figure 8, experimental R_s values as a function of temperature were calculated from both $dV/d\ln(I)$ *vs.* I and $H(I)$ *vs.* I by considering equations (5) and (6), respectively. Both relations gave similar values of R_s where each of these approaches can be used as a control step to check consistency of their results. As presented in figure 8, there is a strong decreasing behaviour in the values of R_s with increasing temperature. This characteristic is related to the factors that affects the increase in n with temperature and lack of free carrier concentration at low temperatures [23].

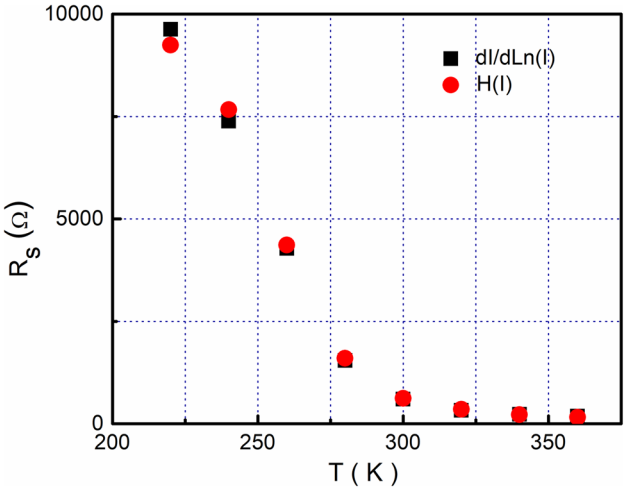

Figure 8. Temperature dependent R_s values of the In/CZTTe/Si/Ag diode.

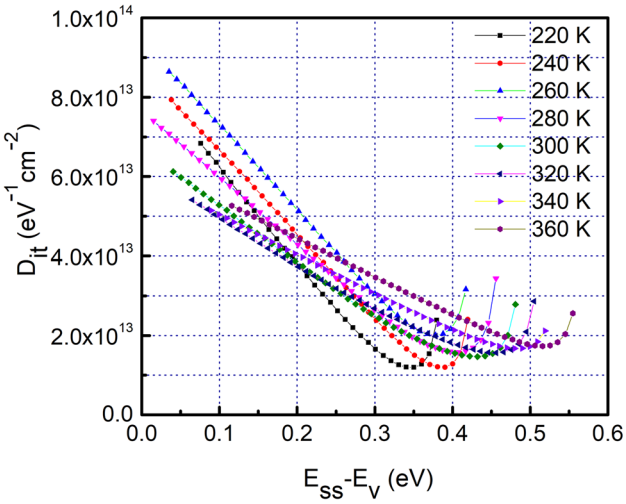

Figure 9. N_{ss} profile for the In/CZTTe/Si/Ag diode.

For the n-type semiconductors, the energy of the interface states E_{SS} from the lower edge of the conductance band at the semiconductor surface is given by,

$$E_C - E_{ss} = q(\Phi_e - V) \tag{7}$$

where the effective barrier height Φ_e is a voltage dependent parameter with the possibility of an interface state in the diode [13–15] and it is expressed by,

$$\Phi_e = \Phi_{B0} + \left(1 - \frac{1}{n\,(V)}\right)(V - IR_s). \tag{8}$$

Therefore, without considering the effect of R_s, N_{ss} values were calculated in terms of $E_C - E_{SS}$. The results are listed in table 1 and also illustrated in figure 9 as a plot of N_{ss} *vs.* $E_C - E_{SS}$. From the density distribution curves of the interface states, the experimental data were found in decreasing behaviour with increasing temperature. This result can be related to the thermal restructuring and reordering of the interface [31].

The observed abnormal deviation from standard TE theory can also be investigated according to the assumption of a spatial fluctuation of the barrier height at the interface [28, 32,33]. Under the assumption of Gaussian distribution (GD) of barrier height, the current flow was discussed in terms of a number of parallel diodes of different Φ_{B0} values, contributing the flow independently [13]. GD of Φ_{B0} was modelled with the mean value and standard deviation, $\bar{\Phi}_{B0}$ and σ_0, respectively. Both parameters of these diodes are voltage and temperature dependent. Then, the I–V relation can be expressed using the following relation by taking into the account the modified barrier height in equation (4) [32,33]:

$$I(V) = AA^*T^2\exp\left[-\frac{q}{kT}\left(\bar{\Phi}_B - \frac{q\sigma_0^2}{2kT}\right)\right] \times\exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \tag{9}$$

by using the saturation current as,

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{ap}}{kT}\right) \tag{10}$$

where Φ_{ap} and n_{ap} are the apparent barrier height and ideality factor, respectively. This relation, given in equation (9), is derived from the approximations with the fact that there is a linear relationship between barrier height and temperature dependence of σ_0 which is negligibly small [33,34]. Thus, the temperature dependence of barrier height under the Gaussian assumption can be expressed as zero-bias apparent barrier height Φ_{ap}:

$$\Phi_{ap} = \bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2KT} \tag{11}$$

with Φ_{B0} and σ_0 values. According to this model, the observed change in the ideality factor with temperature is given as [35],

$$\left(\frac{1}{n_{ap}} - 1\right) = \rho_2 - \frac{q\rho_3}{2kT}. \tag{12}$$

In equation (12), ρ_2 and ρ_3 are named voltage deformation coefficients of the Gaussian parameters $\bar{\Phi}_B$ ($\bar{\Phi}_B = \bar{\Phi}_{B0} - \rho_2 V$) and σ_0 ($\sigma_0 = \sigma_{s0} + \rho_3 V$), respectively [13,14, 36]. The Φ_{ap} *vs.* $q/2kT$ plot is shown in figure 10a to analyse the experimental data under the relation in equation (11), where the straight line behaviour is expected with intercept at the axis of ordinate determining $\bar{\Phi}_{B0}$ and slope giving σ_0. The fitting process to the experimental values was used to

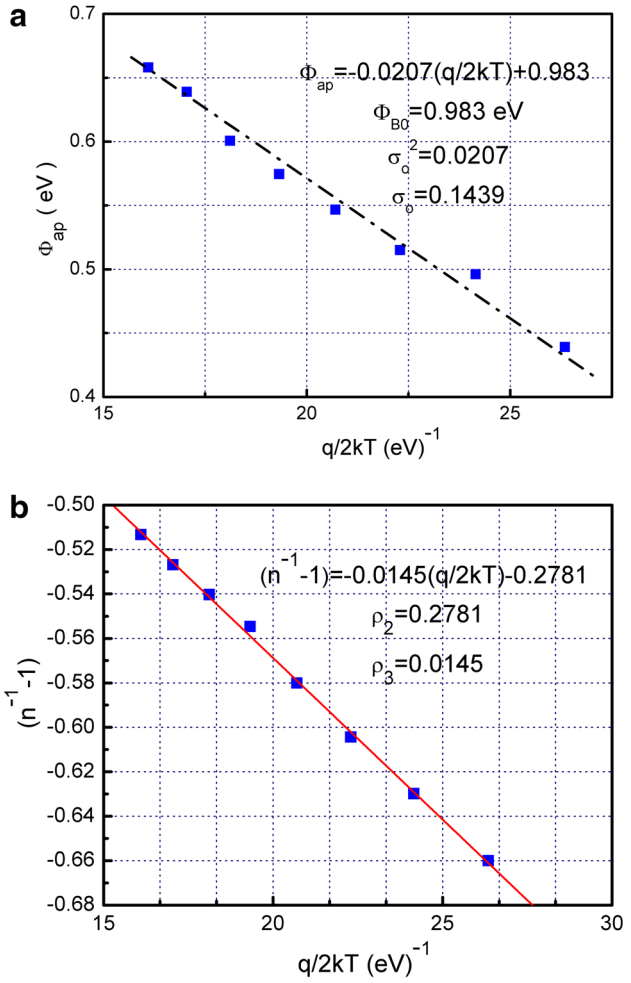

Figure 10. (**a**) Φ_{ap} and (**b**) n_{ap} as a function of $q/2kT$ for the In/CZTTe/Si/Ag diode.

estimate these values as 0.844 and 0.132 eV, for $\bar{\Phi}_{B0}$ and σ_0, respectively. The value of σ_0 is not small compared with the obtained $\bar{\Phi}_{B0}$ and this fact can also indicate the presence of interface inhomogeneity in the fabricated diode structure [33].

For the further analysis of n, the voltage deformation coefficients were determined from the $(n^{-1} - 1)$ *vs.* $q/2kT$ plot in figure 10b. The straight line obtained from the plot gave the values as $\rho_2 = 0.2781$ and $\rho_3 = 0.0145$. As a result of the GD model, the modified Richardson plot can be used to determine $\bar{\Phi}_{B0}$ and A^*, with the slope and intercept values of the plot where the linear relation is expressed as [33],

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\bar{\Phi}_{B0}}{kT}. \qquad (13)$$

In figure 10, from the linear fitting process, the calculated value of $\bar{\Phi}_{B0}$ was in close agreement with the result of equation (11) (see figure 10a). However, there is a significant alteration in A^* values found from the straight line in figures 7 and 11 and the obtained result in figure 11 matches with the expected values in the literature [11].

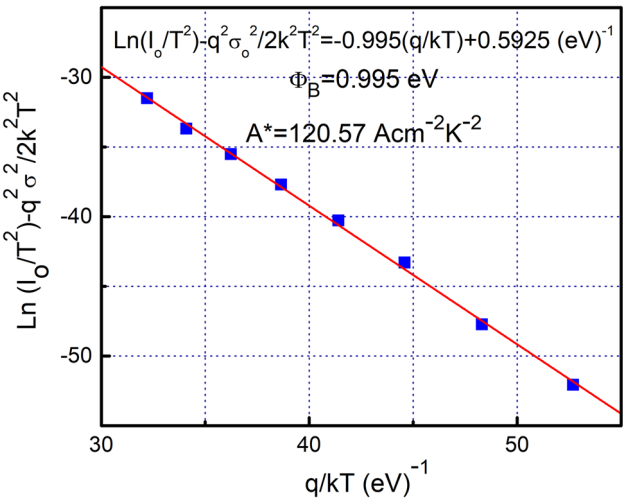

Figure 11. Modified Richardson plot for the In/CZTTe/Si/Ag diode.

4. Conclusion

In this study, temperature-dependent I–V characteristics of the In/CZTTe/Si/Ag sandwich diode structure were investigated in a wide temperature range of 220–360 K. According to the TE model, I_0, Φ_{B0} and n values were calculated for each temperature step and the further analysis was carried out to determine the result of the deviation in the TE model for the high n values than unity and change in the Φ_{B0} with temperature. The experimental values of Φ_{B0} were showed an increasing behaviour with increase in temperature while those of n were decreased with increase in temperature. The total current flow through the diode was modelled by assuming GD of barrier height as a result of inhomogeneous barrier height formation by the presence of the interfacial layer and non-uniformity of the interfacial charge distribution. Additionally, the Richardson plot of saturation current was found in a non-linear behaviour confirming inhomogeneity in the barrier height. Therefore, the modified Richardson plot was used to extract the experimental A^* value. The obtained $\bar{\Phi}_{B0}$ and A^* values confirm the validity of the used TE model modified with the GD of inhomogeneous barrier height. The values of R_s were calculated from the high voltage region by using Cheung functions and N_{ss} values were discussed as a function of $E_C - E_{ss}$.

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