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Reconstructive sensing circuit for complementary resistive switches-based crossbar memories

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Abstract: Complementary resistive switches (CRSs) are suggested as an alternative to one-cell memristor memories to decrease leakage currents. However, their sensing is more difficult and complex than one-cell memristor memories. A method has been given for sensing their state using only DC voltages in the literature. However, in this strategy, sensing one of the logic states results in the destruction of the state and the destroyed state must be written again. To the best of our knowledge, a circuit with this sensing strategy does not exist in the literature yet. In this paper, such a circuit employing this method, which is able to read the CRS cells and able to reconstruct their data if the data are destroyed, is given. A new CRS model is also constructed in this paper and used for simulations to verify the operation of the circuit. The circuit is simulated using Simulink. We expect this circuit implementation to find use in the design and testing of CRS cells.

Key words: Memristor, complementary resistive switches, CRS model, sensing circuits, resistive RAM, crossbar memory

1. Introduction

Memristors and memristive systems are under consideration for nontraditional memory applications [1–3]. They may help to speed up the booting process of computers and may open the way for highly dense memories. Design, optimization, and minimization of their leakage current and power loss are active research areas [3–8]. Complementary resistive switches (CRSs) have been suggested as a way to decrease leakage current and power loss of the memristive crossbar memories [9–17].

The reading of CRS cells may employ different techniques than the one-memristor cells. The sensing technique in [5] cannot be used for CRS cells. A CRS cell with a reading line to ease reading was suggested in [11]; however, it is hard to implement for high-density memories. New architecture or reading techniques are needed for sensing the CRS cells to overcome these difficulties. A new technique to read CRS cells was given and explained in [9]. This technique uses a unipolar voltage to read the CRS state. It predicts the CRS state based on its current. If the initial CRS state is logic 1, unipolar voltage reading results in destruction of the CRS state [9] and the destroyed state should be rewritten to the CRS again. This new technique is simple. However, to the best of our knowledge, a circuit for sensing the CRS cell state automatically with this technique has not been given in the literature yet. In this paper, a sensing circuit for the CRS cell reading strategy is

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designed using combinational logic and an op-amp comparator. The paper is arranged as follows. In the second section, a CRS cell and the sensing strategy given in [9] are briefly explained. In the third section, a new CRS model with nonlinear dopant drift is made. In the fourth section, the sense circuit for the CRS cell, which is designed using a state machine, is given. In the fifth section, the simulation results obtained using MATLAB for the circuit are given. The paper is concluded with the sixth section.

2. Complementary resistive switches

In this section, the CRS cell in [9] is briefly explained. It is redrawn in Figure 1. A resistive switch made of a solid electrolyte sandwiched between platinum and copper electrodes is called the resistive switch U and shown in Figure 1a. Its idealized pinched hysteresis loop is shown in Figure 1b. Another resistive switch made the same way but with opposite polarity is called the resistive switch L and shown in Figure 1c. Its hysteresis loop is shown in Figure 1d. A CRS cell is made by ordering the electrodes and electrolytes in the way shown in Figure 1e. Its equivalent circuit is a pair of antiseries connected resistive switches U and L as shown in Figures 1e. The idealized zero-crossing hysteresis curve of the complementary resistive cell is shown in Figure 1f.

When a memristive element has high resistance, it is in a high resistance state (HRS), and when it has low resistance, it is in a low resistance state (LRS). If the upper memristive element, resistive switch U, is in HRS and the lower memristive element is in LRS, the CRS state is logic 0.

When resistive switch U is in LRS and resistive switch L is in HRS, the CRS state is logic 1. The equivalent CRS memristance or resistance is a little higher than HRS or almost equal to HRS because of the high ratio between HRS and LRS. When a voltage whose magnitude is less than the threshold voltage V_{th1} is applied to the CRS cell, it has a low current and does not switch its state since it is in HRS.

When the initial CRS state is logic 0 and a read voltage that is larger than V_{th1} is applied to the CRS, a very small current is withdrawn by the CRS cell and its logic state does not change, as shown in Figure 2. However, if the CRS is in logic 1 state and then a read voltage larger than V_{th1} is applied to the CRS, a higher current is withdrawn and the state of the CRS cell is destroyed, and it is in logic 0 now. That is why it needs to be written as logic 1 again, as shown in Figure 2.

The logic states of the complementary resistive cell are given in Table 1 [9]. According to [9], state 'ON' occurs only during the read operation. State 'OFF' is the initial state without further importance for the operation and is present only after fabrication. The states '0' and '1' are the memory states for which the equivalent resistance of the CRS is the same.

Table 1. CRS states.

CRS state	Memristor U	Memristor L	Memristance of CRS
Logic 0	HRS	LRS	≈HRS
Logic 1	LRS	HRS	≈HRS
On state	LRS	LRS	LRS + LRS
Off state	HRS	HRS	HRS + HRS

The experimental CRS currents given in [9] are acquired point by point and shown in Figure 2. A reading voltage of 1.25 V (V_{read}), a writing voltage of 5 V to write logic 0, and a writing voltage of –7 V to write logic 1 were used in [9]. Now the CRS cell currents and CRS states as a function of applied voltages are to be explained.

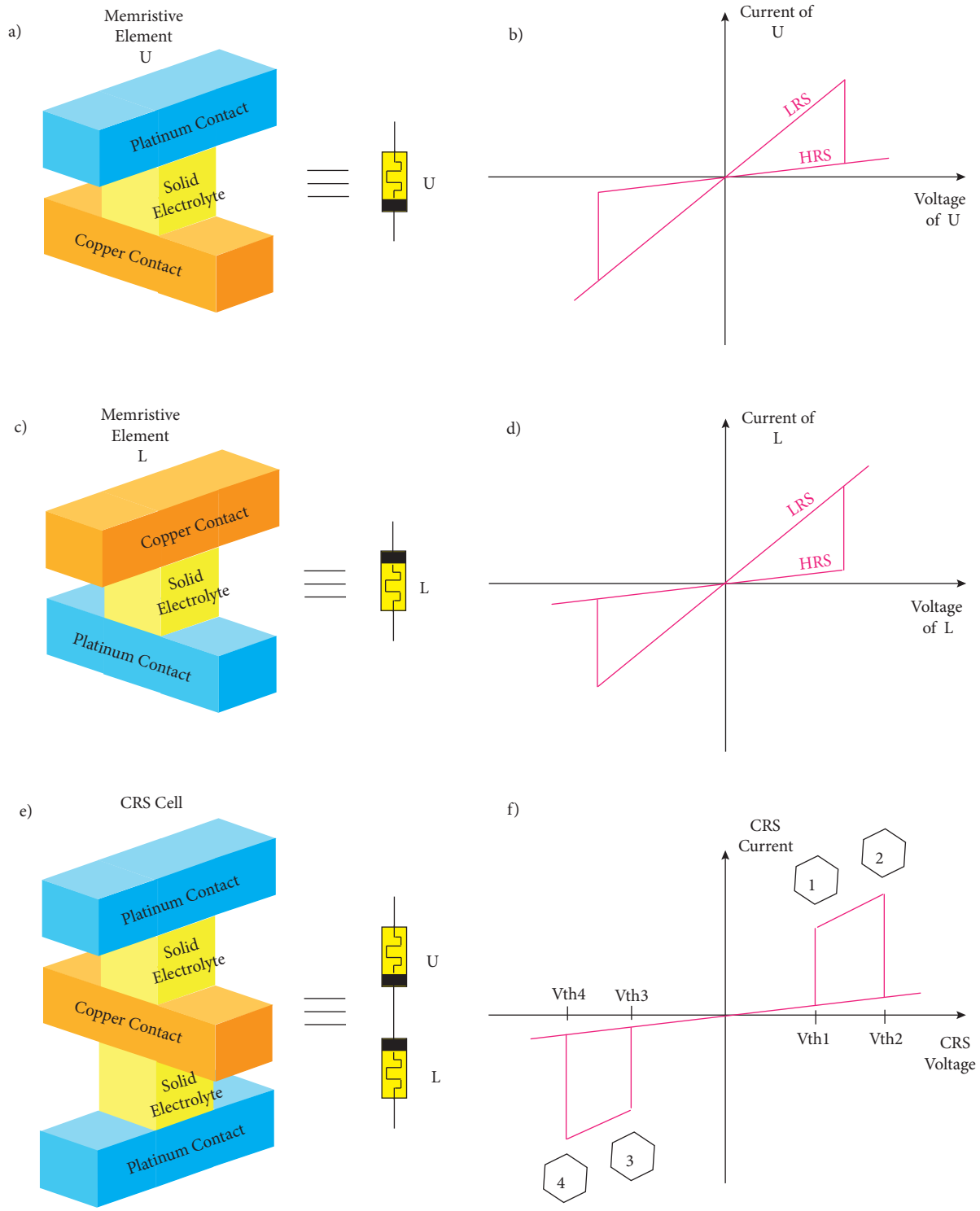

Figure 1. a) The upper memristive element, resistive switch U. b) Zero-crossing hysteresis loop of the upper resistive switch, U. c) The lower memristive element, resistive switch L. d) Zero-crossing hysteresis loop of the lower resistive switch L. f) The complementary resistive switch (CRS), which is made of the antiseries connected memristive elements U and L.

As shown in Figure 2a, if the initial state of the CRS cell is logic 0 and a reading signal is applied, the CRS draws a low current. If the state of the CRS cell is logic 0 and a writing signal of 5 V is applied, the CRS

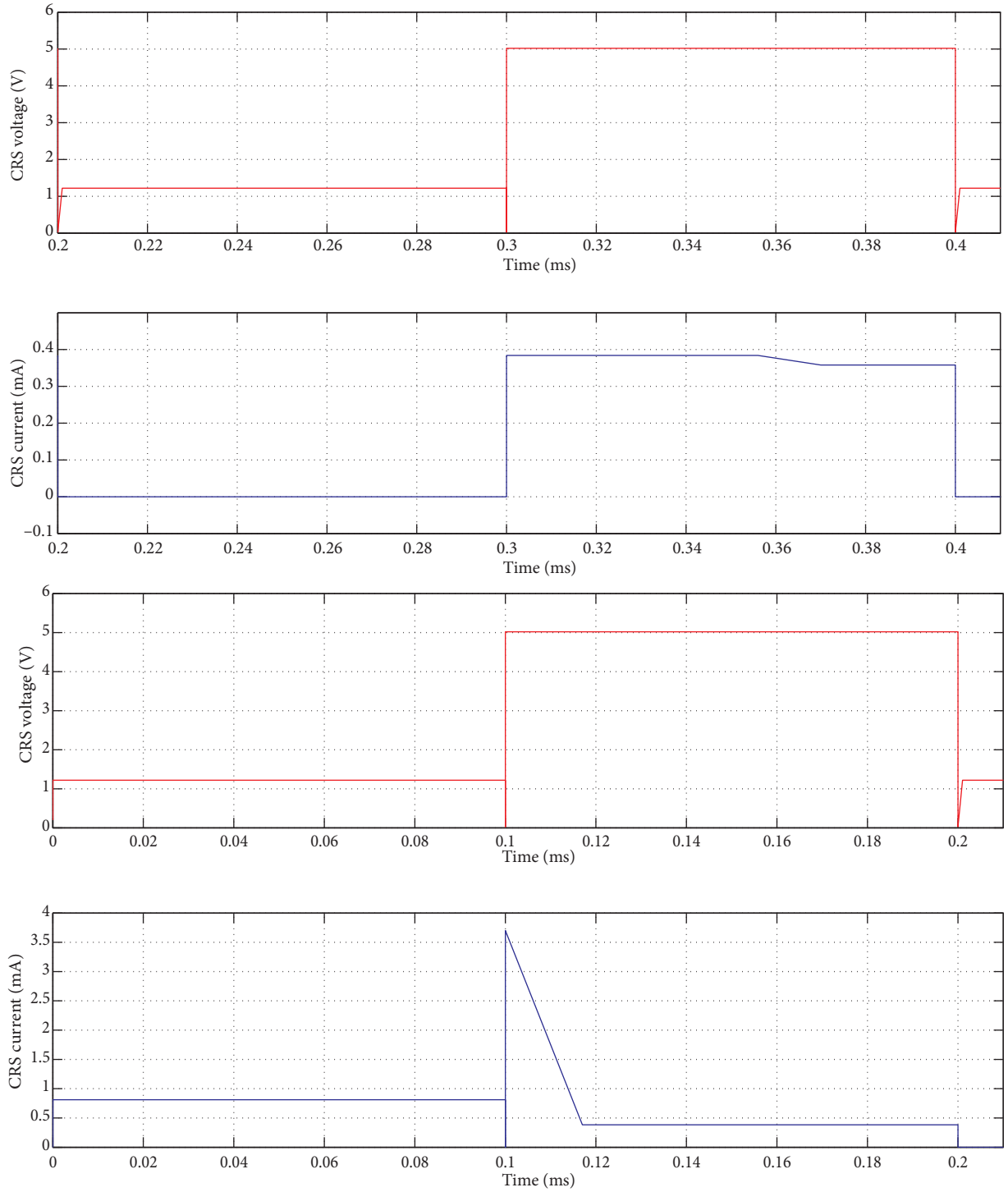

Figure 2. CRS currents reproduced by taking from Figure 2 in [9] point by point.

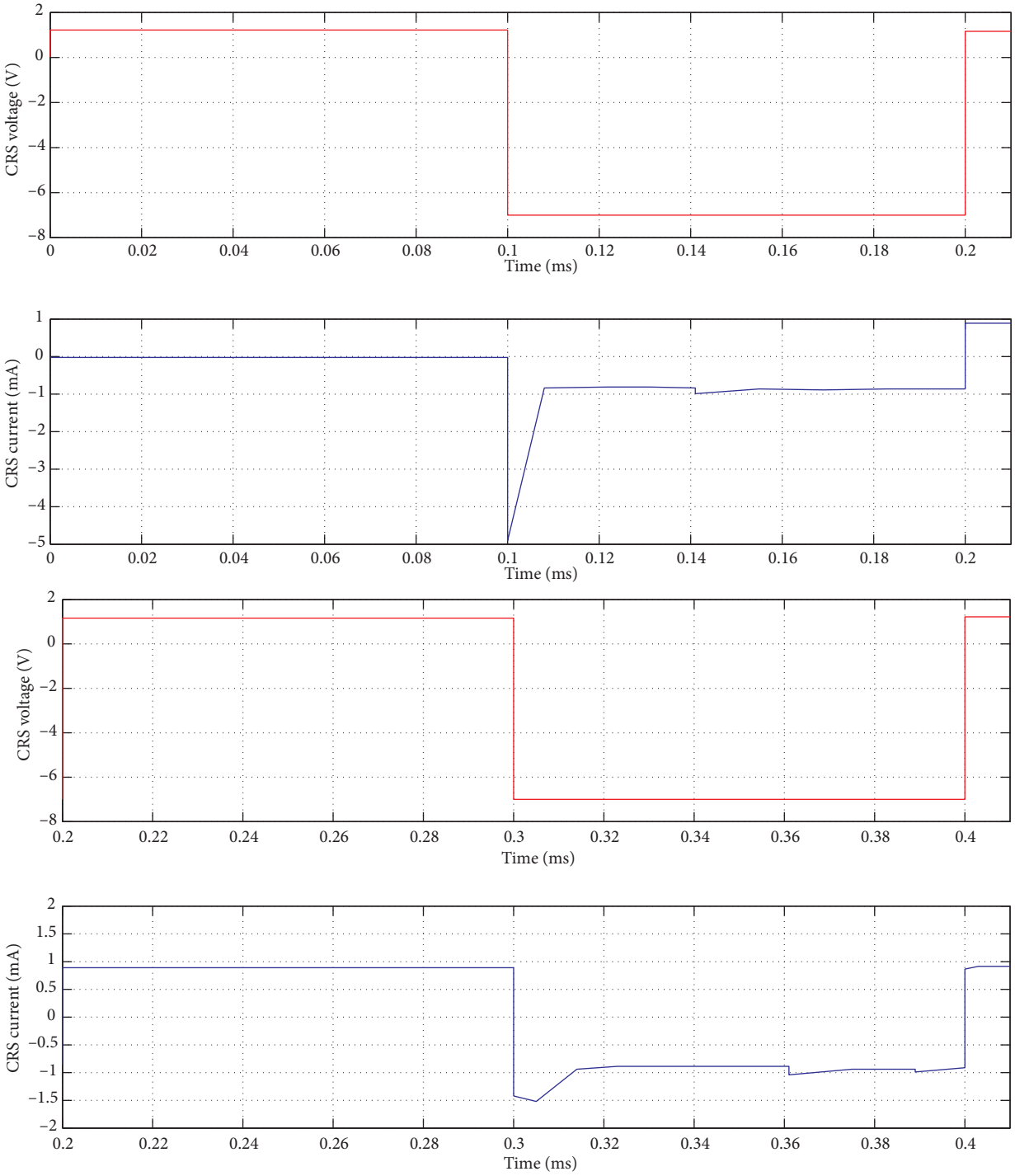

Figure 2. Continued.

draws a relatively high current but its state stays logic 0, and if a reading signal is applied again, it still draws a small current, as shown in Figure 2a.

As shown in Figure 2b, if the initial state of the CRS cell is logic 1 and a reading signal is applied, the CRS draws a high current and its state is destroyed. That means that memristive elements U and L both have

LRS states now. If a writing signal of 5 V is applied, the CRS draws a higher current and its state becomes logic 0, and if a reading pulse is applied again, it draws a small current negligible compared to the writing current as shown in Figure 2b.

If the initial state of the CRS cell is logic 0 and a reading signal is applied, the CRS cell draws a low current and its state stays the same as shown in Figure 2c. That means that the states of the memristive elements U and L do not change. If a writing signal of –7 V is applied, the CRS draws a high current and its state becomes logic 1, and after that short period it draws a small current negligible compared to the writing current of –7 V when it is read again, as shown in Figure 2c.

If the initial state of the CRS cell is logic 1 and it is read, the CRS state is destroyed. High CRS current means that memristive elements U and L both have LRS states now. When a voltage of –7 V is applied to the CRS cell, the CRS draws a high current and its state become logic 1, as shown in Figure 2d. If it is read again, its state is destroyed again.

As shown in Figure 2, a reading of logic 1 destroys the state of the CRS cell and both memristive elements U and L become LRS. In [9], it was suggested that after the destructive reading of logic 1, the CRS cell should be rewritten with –7 V to make its state logic 1 again. A circuit for sensing the CRS cell state and able to reconstruct automatically a destroyed state after sensing with this technique is given in Section 4.

3. Complementary resistive switches model

In this section, a new CRS model is given. The model is inspired from that in [15] and the parameters given in [15] are used in all simulations. The model made in this paper has five voltage ranges to define the rate of change of the normalized dopant drift length using two threshold voltages and also uses two window functions.

The CRS cell equivalent circuit can be seen in Figure 3. The resistive switches are antiseries connected. Therefore, the CRS current is

$$i_{mem} = \frac{V}{R_1 + R_2} = \frac{V}{R_{eq}}, \tag{1}$$

where R_1 and R_2 are the instantaneous upper and lower resistive switch resistances, respectively. The resistances or the memristances of the resistive switches are given as

$$R_1 = R_{on}.x_1 + R_{off}\left(1 - x_1\right) \tag{2}$$

and

$$R_2 = R_{on}.x_2 + R_{off}\left(1 - x_2\right), \tag{3}$$

where x_1 and x_2 are the normalized doped region lengths of elements U and L, respectively. They are equal to

$$x_1 = \frac{w_1}{D} \text{ and } x_2 = \frac{w_2}{D},$$

where w_1 and w_2 are doped region lengths, and D is the length of the resistive switches or the memristive elements.

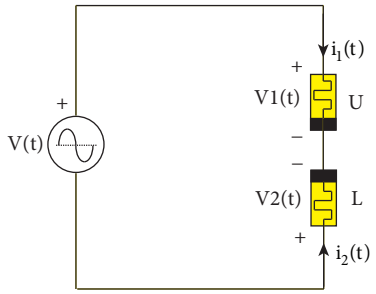

Figure 3. The CRS equivalent circuit.

The currents of the CRS elements are related as

$$i_2(t) = -i_1(t). \tag{4}$$

The window function in [18] is used in this model instead of the one given in [15] and it is given as

$$f(x) = 1 - (x - stp(-i))^{2p}, \tag{5}$$

where x is the normalized doped region length, i is the resistive element current, and p is the window function power parameter.

The window function is not actually a one-variable function as given in the literature; rather, it is a two-variable function. That is why it should be written as

$$f(x, i) = 1 - (x - stp(-i))^{2p}. \tag{6}$$

Since we have two complementary resistive switches, their window functions are

$$f(x_1, i_1) = 1 - (x_1 - stp(-i_1))^{2p} \tag{7}$$

and

$$f(x_2, i_2) = 1 - (x_2 - stp(-i_2))^{2p} = 1 - (x_2 - stp(i_1))^{2p}. \tag{8}$$

In our opinion, considering the hysteresis loop in [9], the rate of change of the state variables are better presented using two threshold voltages as follows.

$$\frac{dx_1}{dt} = \begin{cases} \frac{\mu_v . i_1(t) . R_{off}}{D^2} f(x_1, i_1) & , \quad V_{TH2} \leq V \\ 0 & , \quad V_{TH1} \leq V < V_{TH2} \\ 0 & , \quad -V_{TH1} < V < V_{TH1} \\ \frac{\mu_v . i_1(t) . R_{off}}{D^2} f(x_1, i_1) & , \quad V_{TH2} < V \leq -V_{TH1} \\ 0 & , \quad V \leq -V_{TH2} \end{cases} \tag{9}$$

and

$$\frac{dx_2}{dt} = \begin{cases} 0 & , \quad V_{TH2} \leq V \\ \frac{\mu_v . i_2(t) . R_{off}}{D^2} f(x_2, i_2) & , \quad V_{TH1} \leq V < V_{TH2} \\ 0 & , \quad -V_{TH1} < V < V_{TH1} \\ 0 & , \quad V_{TH2} < V \leq -V_{TH1} \\ \frac{\mu_v . i_2(t) . R_{off}}{D^2} f(x_2, i_2) & , \quad V \leq -V_{TH2} \end{cases} \tag{10}$$

The reason why the equivalent CRS resistance, $R_{eq} = R_1 + R_2$, is not constant are the switches' threshold voltages and window functions. We could not acquire the CRS parameters from the data given in [9] since the

frequency of the hysteresis loop in [9] was not given. That is why the CRS parameters taken from [15] and given in Table 2 are used in this and the next section.

Table 2. The CRS parameters used in the simulations.

The minimum resistance value of one memristive element	R_{on}	3.16 kΩ
The maximum resistance value of one memristive element	R_{off}	316 kΩ
The window function power	P	2
The dopant mobility in the memristive element	μ_v	0.0017827 $\frac{m^2}{V.s}$
The memristive element length	D	0.13 μm
The first positive threshold voltage	$V_{th1} = -V_{th3}$	0.58 V
The second positive threshold voltage	$V_{th2} = -V_{th4}$	1.3 V

The zero-crossing hysteresis curve of the CRS excited with a voltage source of $V(t) = V_m \cos(\omega t) = 1.4\cos(20{,}000\,\pi t)$ is shown in Figure 4. The CRS current and voltage are given in Figure 5. The resistive switching of the complementary switches can be seen in Figure 6. The CRS model is used in the fifth section to prove the reconstructive sensing circuit concept.

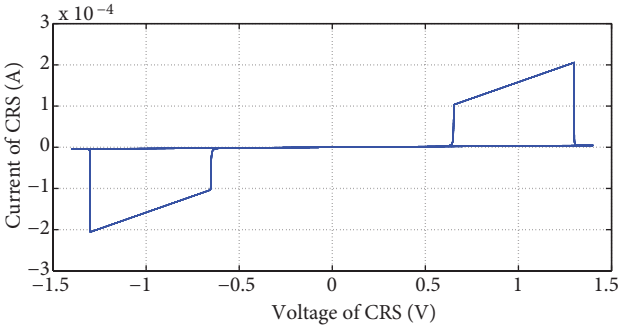

Figure 4. The zero-crossing hysteresis loop of the CRS model when excited with $V(t) = V_m \cos(\omega t) = 1.4\cos(20{,}000\,\pi t)$.

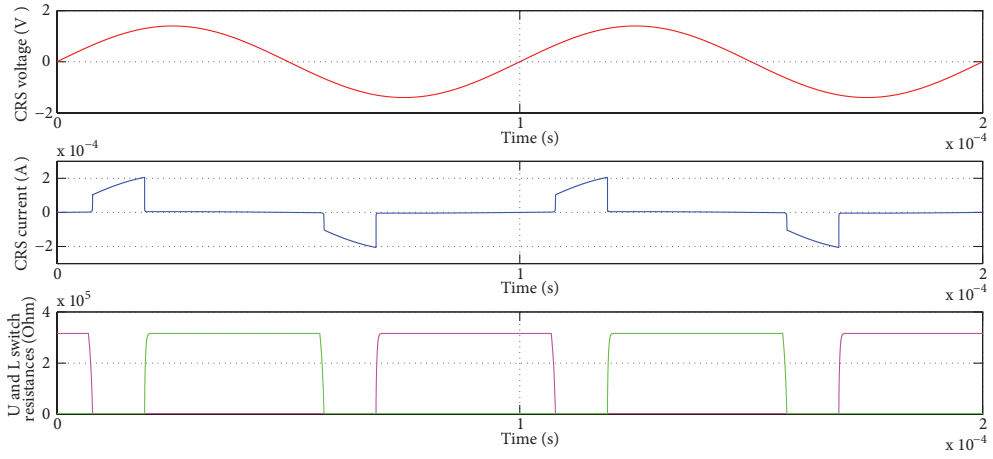

Figure 5. The CRS current and voltage when excited with $V(t) = V_m \cos(\omega t) = 1.4\cos(20{,}000\,\pi t)$.

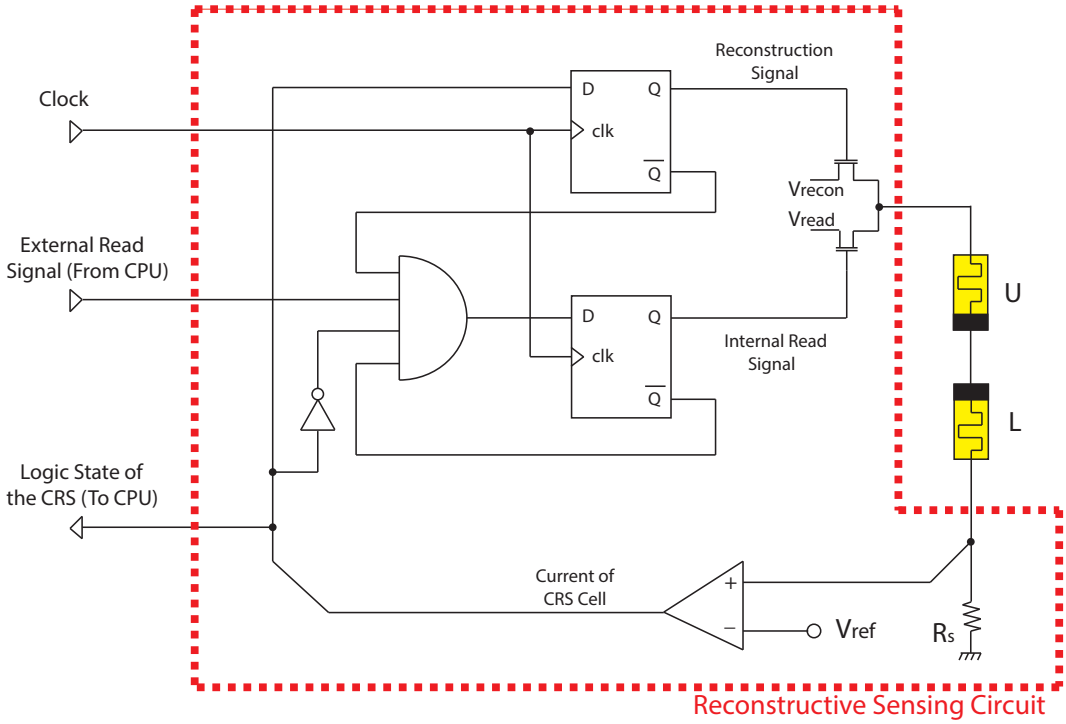

Figure 6. Proposed reconstructive sensing circuit (RSC).

4. Reconstructive sensing circuit

In this study, a reconstructive sensing circuit (RSC) is designed and it is explained in the following section. The designed sensing circuit is shown in Figure 7. Resistor R_s is connected in series to the CRS to sense the complementary resistive cell current. An op-amp is used as a comparator as shown in Figure 7. It compares the voltage across the sense resistor, which is proportional to the complementary current to a predefined reference voltage, $\mathbf{V_{ref}}$. If the read voltage is applied and the lower memristor's initial state is logic 1, the CRS draws a high current, the positive input of the comparator becomes higher than the reference voltage, the output of the comparator becomes logic 1, and the state of the memristor is destroyed. If the read voltage is applied and the lower memristor's initial state is logic 0, the CRS draws a low current, the positive input of the comparator becomes lower than the reference voltage, the output of the comparator becomes logic 0, and the state of the memristor stays the same. The comparator output is also the logic state of the CRS cell or the initial data within the CRS are read and sent out to the CPU for processing. The comparator reference voltage should be chosen considering the following criteria. During reading of CRS state logic 0,

$$V_{ref} > \frac{R_s}{R_{HRS} + R_{LRS} + R_s}.V_{read}, \tag{11}$$

and during reading of CRS state logic 1,

$$V_{ref} < \frac{R_s}{R_{LRS} + R_{LRS} + R_s}.V_{read}. \tag{12}$$

However, the best choice of R_s might be made experimentally due to the leakage currents of the CRS memory arrays.

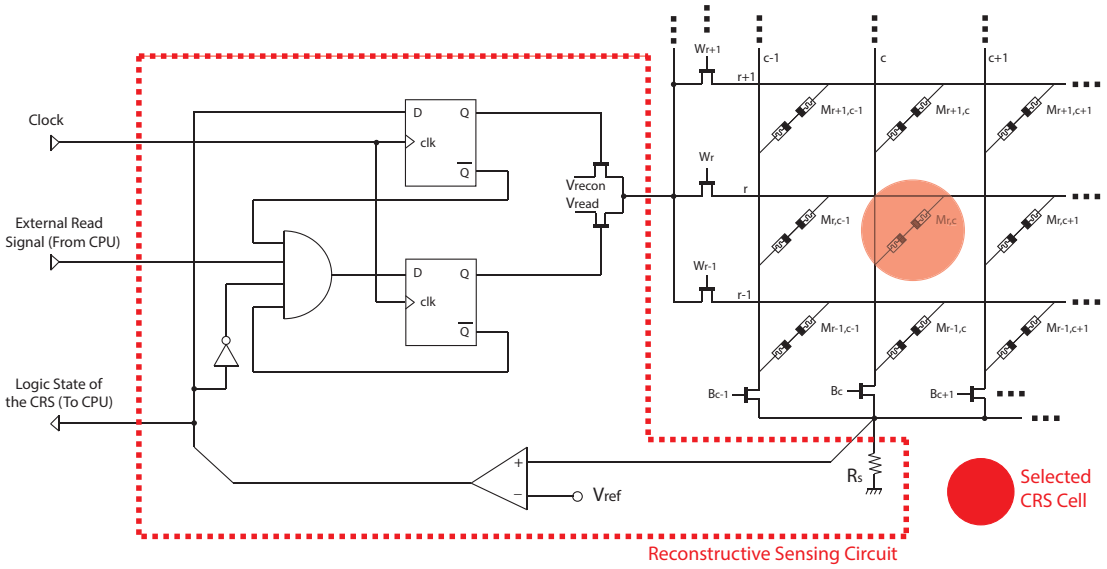

Figure 7. Combined RSC and CRS crossbar memory.

A state-machine with D-type flip-flops is designed for the sensing circuit. The state-machine has two inputs, the clock signal and the external read signal. It has three outputs, the internal read signal, the reconstruction signal, and the logic state of the CRS cell. The reconstruction signal controls the reconstruction signal $\mathbf{V_{recon}}$ (–4 V) and the other output, the internal read, controls the reading voltage $\mathbf{V_{read}}$ (1.25 V). The connection of the RSC to the CRS cell is also shown in Figure 7.

The state-machine takes the external read signal from the CPU, produces the internal read signal, and applies it to a MOSFET to supply $\mathbf{V_{read}}$ to the CRS cell at the first coming clock cycle. The reconstruction signal is logic 0 unless the data in the CRS are not destroyed.

In just one clock cycle, the state-machine senses the state of the CRS cell. The state-machine is designed in such a way that it is able to reconstruct the destroyed data in the next clock cycle. If the CRS data are destroyed, at the next clock signal, it activates a write signal of –4 V to reconstruct the destroyed state of logic 1. The state-machine is able to reconstruct the destroyed data in the CRS cell and also continues to reconstruct data even if the external read signal ends prematurely. The RSC circuit can be combined with a CRS crossbar memory array as shown in Figure 8. A half-selection method is also used for the CRS crossbar memory array as in [14,15].

5. Simulation results

In this section, simulations are done to show the RSC concept using the Simulink toolbox of MATLAB. The simulation results of the RSC are given in Figures 8 and 9. The results show that the circuit is able to sense the state of the CRS cell.

If the CRS initial state is logic 0 and an external read signal comes, at the next coming clock cycle, the logic state of the CRS becomes logic 0, the CRS draws a low current, the CRS state is not destroyed, and the reconstruction signal is logic 0 since the data in the CRS are not destroyed, as shown in Figure 8.

If the CRS initial state is logic 1 and the CRS is read, the CRS data are destroyed as shown in Figure 9. After the destruction of the CRS state, at the next clock signal, it activates a write signal of –4 V to reconstruct the destroyed state of logic 1, and the RSC is able to reconstruct the destroyed data even though the external read signal ends prematurely as seen in Figure 9.

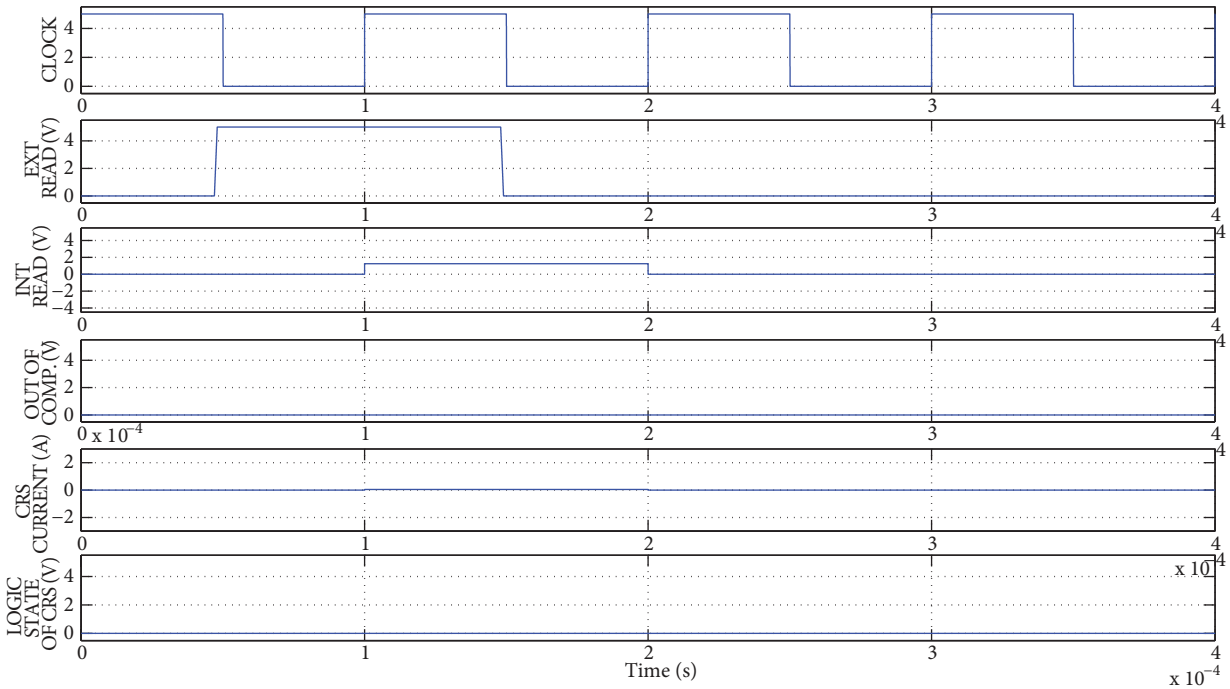

Figure 8. Sensing circuit signals circuit when the initial logic state of CRS is '0'.

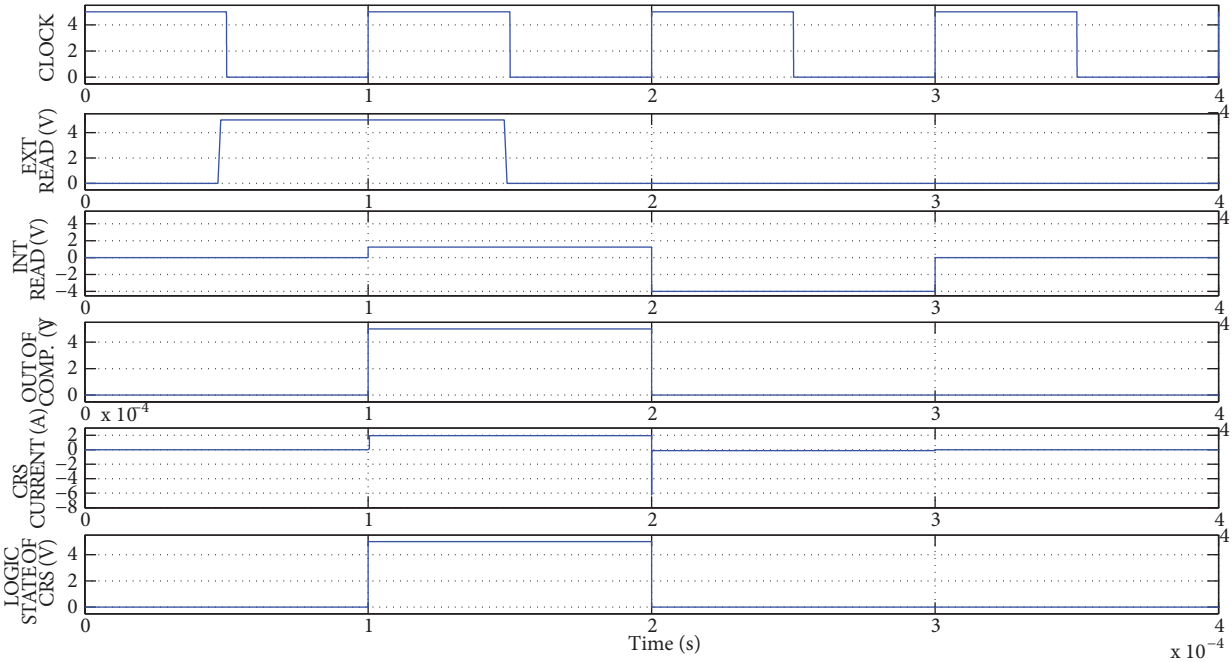

Figure 9. Sensing circuit signals circuit when the initial logic state of CRS is '1'.

If the waveforms given in Figures 2 and 9 are compared, it can be seen that the current variation or the current spikes seen in Figure 2 cannot be predicted with either the CRS model in [15] or the model given here. The reason for this might be that, in [19], the memristive devices were claimed to be of stochastic nature and while individual switching events are random, the distribution and probability of switching can be predicted

well and controlled. That means that individual CRS current spikes are random and cannot be predicted very accurately due to the significant randomness or temporal variations experienced during normal operations [20,21]. None of the CRS models in the literature are stochastic, i.e. all of them are deterministic. There may be a need for making a CRS model of stochastic nature considering the random nature of switching events. However, the CRS model given here is good enough and able to produce a hysteresis loop similar to the one given in [9], and it is able to demonstrate RSC operation.

6. Conclusion

We have designed a circuit to sense the CRS cells with the technique given in [9]. A combinational circuit is used to reconstruct the destroyed CRS data using the read current of the CRS cell and clock signal.

A new CRS model is made to show the operation of the circuit. Both the CRS model and reconstructive sensing circuit are simulated using the Simulink toolbox of MATLAB.

If the CRS data are not destroyed, the reading just takes one cycle. The reading operation at worst just takes two clock cycles with this circuit. Therefore, the reading speed is half of the writing speed for the CRS cell. The reading time of logic 0 is just half of the reading time of logic 1 since there is no reconstruction occurring for the initial state of logic 0. If in the future CRS array memories become more common, CPU topologies may also be modified for the different reading speeds of the CRS array memories considering their different logic states to decrease operation time. For example, a logic input can be added to CPUs using the CRS memory arrays to know the reconstruction status and therefore speed up reading of the CRS memory arrays.

It is our belief that such a reconstructive sensing circuit may be used for reading CRS cells and become an integrated part of CRS memories in the future.

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